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[File 348] EUROPEAN PATENTS 1978-200848
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[File 349] PCT FULLTEXT 1979-2008/UB=20081120|UT=20081113
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Set     Items   Description
S1      61929   S (COMPRESS? OR ZIP? ? OR ZIPPED OR ZIPPING OR STUFF??? OR WINZIP? OR SQUEEZ? OR
COMPACT???)(5N)(DATA OR DATUM OR FILE? ? OR INFORMATION OR CONTENT? ? OR RECORD? ? OR
DATABASE? OR DATA()BASE? OR REPOSITOR? OR RESOURCE? ?)
S2    1659156   S (FILL????? OR MERGE?? OR MERGING OR POPULATE? OR COMPLET??? OR SUPPLY??? OR
FURNISH???)
S3       6537   S S2(3N)(RANDOM?? OR PSEUDO()RANDOM?? OR PSEUDORANDOM?? OR ARBITRAR??? OR
CHANCE OR DISCRETIONAR? OR AD()HOC OR UNSYSTEMATIC?)
S4    2128370   S (VECTOR? ? OR PATTERN? ? OR BIT? ? OR BYTE? ? OR SEQUENCE? ? OR SERIES OR
STRING? ? OR DATA OR INFORMATION OR SIGNAL? ? OR CHARACTER? ? OR INPUT? ? OR SEGMENT? ? OR
PROGRAM? ? OR VALUE? ?)
S5         12   S S2(5N)(CARE(2W)(BIT? ? OR BYTE? ? OR CODE? ?))
S6         11   S S5(10N)S4
S7          3   S S3(15N)S6
S8     369999   S S4(10N)((LESS OR SMALLER OR LOWER OR LOOSEN OR BELOW OR FEWER OR
MINOR?)(3N)(NUMBER? ? OR NUMERAL? ? OR CHARACTER? ? OR VALUE? ? OR DATA OR INFORMATION OR
FIGURE? ? OR DIGIT? ? OR INTEGER? ? OR BIT? ? OR BYTE? ? OR WORD? ? OR CONTENT? ? OR AMOUNT? ?
OR QUANTIT??? OR PATTERN? ? OR SEQUENCE? ? OR SERIES? ? OR STREAM? ?))
S9          3   S S8(20N)S7
S10        12   S S5(100N)S4
S11         3   S S3(15N)S10
S12         4   S S3(100N)S10

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Subject summary

? t /3,k/all
12/3K/1 (Item 1 from file: 348) Links
Fulltext available through: Order File History
EUROPEAN PATENTS

01838016
DATA COMPRESSION
DATENKOMPRIMIERUNG
COMPRESSION DE DONNEES

Patent Assignee:

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(Proprietor designated states: all)
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Legal Representative:

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NXP Semiconductors Intellectual Property Department Cross Oak Lane; Redhill, Surrey RH1 5HA; (GB)

	Country	Number	Kind	Date	
Patent	EP	1620740	A1	20060201	(Basic)
	EP	1620740	B1	20071031	
	WO	2004097438		20041111	
Application	EP	2004729698		20040427	
	WO	2004IB50520		20040427	
Priorities	EP	2003101186		20030429	

Designated States:
AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; HU; IE; IT; LI; LU; MC;
NL; PL; PT; RO; SE; SI; SK; TR;
Extended Designated States:
AL; HR; LT; LV; MK;
International Patent Class (V7): G01R-031/319

IPC	Level	Value	Position	Status	Version	Action	Source	Office
G01R-0031/319	A	I	F	B	20060101	20041117	H	EP

NOTE: No A-document published by EPO

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application: English

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200744	394
CLAIMS B	(German)	200744	381
CLAIMS B	(French)	200744	449
SPEC B	(English)	200744	5710
Total Word Count (Document A) 0			
Total Word Count (Document B) 6934			
Total Word Count (All Documents) 6934			

Specification: ...i.e. 'care' bits, while most stimulus bits are 'don't care' and can be filled at random. In principle, only the specified stimulus bits have to be stored in the... ...with '0' or '1'. Repeat fill implies that each don't care bit in a sequence is given the same value as the most recent care bit.
For example, consider the sequence 0XX1XX, where the symbol X denotes a don't care bit. Applying a 0- fill to this sequence results in 000100 (i.e. all X's replaced with 0's). Applying a 1-fill to the same sequence results in 011111. Applying repeat fill results in 000111 (i.e. the X's after the 0 and before the 1 are assigned the value 0, whereas the X's after the 1 are assigned the value 1).
Test vectors can be compressed by using the vector repeat capability as supported by most ATE configurations. Figure 1A is a schematic block diagram illustrating a typical ATE architecture. The test vectors are stored in the ATE vector memory 100, while the instruction memory 102 contains instructions as to how to apply these... ...fill allows much higher repeat counts than other padding types, thereby significantly reducing the test data volume required to be stored.

An additional degree of freedom can be achieved by reordering ... ...quality, the don't care bits in incompatible vectors are therefore filled best with random values. Furthermore, if a sequence of compatible vectors is short (i.e., smaller than some value n), then the don't care bits in these vectors can also be filled with random values. If a sequence of compatible test vectors is large (i.e., larger than or equal to n), then merge-fill can be applied to fill the don't care bits in these vectors. The result is that higher test quality is achieved when compared to using merge-fill only, which comes at the cost of slightly reduced test data compression when using run-length encoding, i.e., vector repeat.
These and other aspects of the invention will be apparent from and elucidated with... ...create new merge-vector */)
)</PRE>
Example 1
Referring to the above example, (a) denotes a sequence of 6 test vectors, and (b) shows the merged test vectors that are generated when... ...but some don't care bits have been filled in (e). The remaining don't care bits in the merged test vectors can be filled randomly, as for example, illustrated in (f).
In the above example, storing the original test vector sequence requires storing 6 test vectors. Storing the merged test vector sequence requires storing only 3 merged test vectors, plus the repeat count for each merged test vector. The net effect is a significant reduction of the test data volume for storing this vector sequence.
For unordered pattern sets, the possibility to reorder the test patterns offers an additional degree of freedom. It is preferred to order the patterns in such a way that the last merged test vector of a pattern is compatible with the first merged test vector of the subsequent pattern...

12/3K/2 (Item 2 from file: 348) Links
Fulltext available through: Order File History
EUROPEAN PATENTS

01807636
Data compression
Datenkompression
Compression de donnees

Patent Assignee:

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(Applicant designated States: all)
Inventor:

- The designation of the inventor has not yet been filed

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Legal Representative:

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Philips Intellectual Property & Standards P.O. Box 220; 5600 AE Eindhoven; (NL)

	Country	Number	Kind	Date	
Patent	EP	1475644	A1	20041110	(Basic)
Application	EP	2003101186		20030429	

Designated States:
AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; HU; IE; IT; LI; LU; MC;
NL; PT; RO; SE; SI; SK; TR;
Extended Designated States:
AL; LT; LV; MK;
International Patent Class (V7): G01R-031/319Abstract Word Count: 104
NOTE: 2
NOTE: Figure number on first page: 2

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application: English

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200446	683
SPEC A	(English)	200446	5418
Total Word Count (Document A) 6101			
Total Word Count (Document B) 0			
Total Word Count (All Documents) 6101			

Specification: ...bits is specified (usually only a few percent), i.e. 'care' bits, while most stimulus bits are 'don't care' and can be filled at random. In principle, only the specified... ...with '0' or '1'. Repeat fill implies that each don't care bit in a sequence is given the same value as the most recent care bit.
For example, consider the sequence 0XX1XX, where the symbol X denotes a don't care bit. Applying a 0- fill to this sequence results in 000100 (i.e. all X's replaced with 0's). Applying a 1 -fill to the same sequence results in 011111.

Applying repeat fill results in 000111 (i.e. the X's after the 0 and before the 1 are assigned the value 0, whereas the X's after the 1 are assigned the value 1).
Test vectors can be compressed by using the vector repeat capability as supported by most ATE configurations. Figure 1A is a schematic block diagram illustrating a typical ATE architecture. The test vectors are stored in the ATE vector memory 100, while the instruction memory 102 contains instructions as to how to apply these... ...fill allows much higher repeat counts than other padding types, thereby significantly reducing the test data volume required to be stored.
An additional degree of freedom can be achieved by reordering ... ...quality, the don't care bits in incompatible vectors are therefore filled best with random values. Furthermore, if a sequence of compatible vectors is short (i.e., smaller than some value n), then the don't care bits in these vectors can also be filled with random values. If a sequence of compatible test vectors is large (i.e., larger than or equal to n), then merge-fill can be applied to fill the don't care bits in these vectors. The result is that higher test quality is achieved when compared to using merge-fill only, which comes at the cost of slightly reduced test data compression when using run-length encoding, i.e., vector repeat.
These and other aspects of the invention will be apparent from and elucidated with... ...shortest possible sequence after merging.
Example 1
Referring to the above example, (a) denotes a sequence of 6 test vectors, and (b) shows the merged test vectors that are generated when... ...some don't care bits have been filled in (e). The remaining don't care bits in the merged test vectors can be filled randomly, as for example, illustrated in (f).
In the above example, storing the original test vector sequence requires storing 6 test vectors. Storing the merged test vector sequence requires storing only 3 merged test vectors, plus the repeat count for each merged test vector. The net effect is a significant reduction of the test data volume for storing this vector sequence.
For unordered pattern sets, the possibility to reorder the test patterns offers an additional degree of freedom. It is preferred to order the patterns in such a way that the last merged test vector of a pattern is compatible with the first merged test vector of the subsequent pattern ...
Claims: ...testing a logic product, and the apparatus includes means for generating or receiving original test vector data comprising a sequence of two or more vectors, wherein a vector comprises one or... ...of test vector data comprising a sequence of < n vectors, while said don't care bits are filled by merging compatible vectors in the case of test vector data comprising a sequence of ≥ n compatible vectors.
12. Apparatus according to claim 10, including apparatus according to claim 8 for compressing said output data.
13. Apparatus according to any one of claims 10 to 12, wherein said means for generating original test vector data comprises an Automated Test Pattern Generation (ATPG) tool.
14. Apparatus according to claim 13, including means for reordering a test pattern, prior to compression thereof.
15. Apparatus according to claim 10, including means for storing merged data sequences in the form of a data set for use in testing a logic product.
16. Electronic data storage means on which...

12/3K/3 (Item 1 from file: 349) Links
Fulltext available through: Order File History
PCT FULLTEXT

01313061
METHOD FOR AT LEAST PARTIALLY COMPENSATING FOR ERRORS IN INK DOT PLACEMENT DUE TO ERRONEOUS ROTATIONAL DISPLACEMENT
PROCEDE POUR LA COMPENSATION AU MOINS PARTIELLE D'ERREURS DANS LE PLACEMENT POINTS D'ENCRE DUES A UN DEPLACEMENT ROTATIONNEL ERRONE

Patent Applicant/Patent Assignee:

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Patent Applicant/Inventor:

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	Country	Number	Kind	Date
Patent	WO	2005120835	A1	20051222
Application	WO	2004AU706		20040527
Priorities	WO	2004AU706		20040527

Designated States: (All protection types applied unless otherwise stated - for applications 2004+)
AE; AG; AL; AM; AT; AU; AZ; BA; BB; BG;
BR; BW; BY; BZ; CA; CH; CN; CO; CR; CU;
CZ; DE; DK; DM; DZ; EC; EE; EG; ES; FI;
GB; GD; GE; GH; GM; HR; HU; ID; IL; IN;
IS; JP; KE; KG; KP; KR; KZ; LC; LK; LR;
LS; LT; LU; LV; MA; MD; MG; MK; MN; MW;
MX; MZ; NA; NI; NO; NZ; OM; PG; PH; PL;
PT; RO; RU; SC; SD; SE; SG; SK; SL; SY;
TJ; TM; TN; TR; TT; TZ; UA; UG; US; UZ;
VC; VN; YU; ZA; ZM; ZW;
[EP] AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; HU; IE; IT; LU; MC; NL;
PL; PT; RO; SE; SI; SK; TR;
[OA] BF; BJ; CF; CG; CI; CM; GA; GN; GQ; GW;
ML; MR; NE; SN; TD; TG;
[AP] BW; GH; GM; KE; LS; MW; MZ; NA; SD; SL;
SZ; TZ; UG; ZM; ZW;
[EA] AM; AZ; BY; KG; KZ; MD; RU; TJ; TM;

Publication Language: English
Filing Language: English
Fulltext word count: 618378
Claims:
...on a 256-bit DRAM boundary. If data stored is not a multiple of 256- bits then the last word should be padded.
9 3 CPU subsystem bus addressed registersThe CPU subsystem bus supports 32-bit word aligned read and write accesses with variable access timings. See section 11.4 for...

12/3K/4 (Item 2 from file: 349) Links
Fulltext available through: Order File History
PCT FULLTEXT

01174846
DATA COMPRESSION
COMPRESSION DE DONNEES

Patent Applicant/Patent Assignee:

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Patent Applicant/Inventor:

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- HOLLMANN Hendrik D L
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Legal Representative:

- ELEVELD Koop J(agent)
Prof. Holstlaan 6, NL-5656 AA Eindhoven; NL;

	Country	Number	Kind	Date
Patent	WO	200497438	A1	20041111
Application	WO	2004IB50520		20040427
Priorities	EP	2003101186		20030429

Designated States: (All protection types applied unless otherwise stated - for applications 2004+)
AE; AG; AL; AM; AT; AU; AZ; BA; BB; BG;

BR; BW; BY; BZ; CA; CH; CN; CO; CR; CU;
CZ; DE; DK; DM; DZ; EC; EE; EG; ES; FI;
GB; GD; GE; GH; GM; HR; HU; ID; IL; IN;
IS; JP; KE; KG; KP; KR; KZ; LC; LK; LR;
LS; LT; LU; LV; MA; MD; MG; MK; MN; MW;
MX; MZ; NA; NI; NO; NZ; OM; PG; PH; PL;
PT; RO; RU; SC; SD; SE; SG; SK; SL; SY;
TJ; TM; TN; TR; TT; TZ; UA; UG; US; UZ;
VC; VN; YU; ZA; ZM; ZW;
[EP] AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; HU; IE; IT; LU; MC; NL;
PL; PT; RO; SE; SI; SK; TR;
[OA] BF; BJ; CF; CG; CI; CM; GA; GN; GQ; GW;
ML; MR; NE; SN; TD; TG;
[AP] BW; GH; GM; KE; LS; MW; MZ; NA; SD; SL;
SZ; TZ; UG; ZM; ZW;
[EA] AM; AZ; BY; KG; KZ; MD; RU; TJ; TM;

Publication Language: English
Filing Language: English
Fulltext word count: 6989
Detailed Description:
...1 5 specified (usually only a few percent), i.e. 6care' bits, while most stimulus bits are 'don't care' and can be filled at random. In principle, only the specified... ...data corresponds to 0-fill or 1 -fill, where all of the don't care bits are filled with 'O' or 'I'. Repeat fill implies that each don't care bit in a sequence is given the same value as the most recent care bit. For example, consider the sequence OXX I XX, where the symbol X denotes a don't care bit. Applying a O-fill to this sequence results in 000 I 00 (i.e. all X's replaced with O's). Applying a I -fill to the same sequence results in 0 1 1 1 1 1. Applying repeat fill results in 000 I... ...i.e. the X's after the 0 and before the I are assigned the value 0, whereas the X's after the I are assigned the value 1).
Test vectors can be compressed by using the vector repeat capability as
supported by most ATE configurations. Figure IA is a schematic block diagram... ...allows much higher repeat counts than other padding types, thereby 5 significantly reducing the test data volume required to be stored.
An additional degree of freedom can be achieved by reordering ... ...quality, the don't care bits in incompatible vectors are therefore filled best with random values. Furthermore, if a sequence of compatible vectors is short (i.e., smaller than some value n), then the don't care bits in these vectors can also be filled with random values. If a sequence of compatible test vectors is large (i.e., larger than or equal to n), then merge-fill can be applied to fill the don't care bits in these vectors. The result is that higher test quality is achieved when compared to using merge-fill only, which comes at the cost of slightly reduced test data compression when using run-length encoding, i.e., vector repeat.
These and other aspects of the invention will be apparent from and elucidated with... ...M
I 0 Referring to the above example, (a) denotes a sequence of 6 test vectors, and (b) shows the merged test vectors that are generated when executing the above algorithm... ...but some don't care bits have been filled in (e). The remaining don't care bits in the merged test vectors can be filled randomly, as for example, illustrated in (f).
In the above example, storing the original test vector sequence requires storing 20 6 test vectors. Storing the merged test vector sequence requires storing only 3 merged test vectors, plus the repeat count for each merged test vector. The net effect is a significant reduction of the test data volume for storing this vector sequence.
For unordered pattern sets, the possibility to reorder the test patterns offers an additional degree of freedom. It is preferred to order the patterns in such a way that the last 25 merged test vector of a pattern is...
Claims:
...testing a logic product, and the apparatus includes means for generating or receiving original test vector data comprising a sequence of two or more vectors, wherein a vector comprises one or... ...of test vector data comprising a sequence of <n vectors, while said don't care bits are filled by merging compatible vectors in the case of test vector data comprising a sequence of >n compatible vectors.
12 Apparatus according to claim 10, including apparatus according to claim 8 for compressing said output data.
13 Apparatus according to any one of claims IO to 12, wherein said means for generating original test vector data comprises an Automated Test Pattern Generation (ATPG) tool.
5
14 Apparatus according to claim 13, including means for reordering a test pattern, prior to compression thereof.
15 Apparatus according to claim 10, including means for storing merged data 10 sequences in the form of a data set for use in testing a logic product. I 6. Electronic data storage means on...

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